

74F194 4-Bit Bidirectional Universal Shift Register

General Description

The 74F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed, multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers.

Features

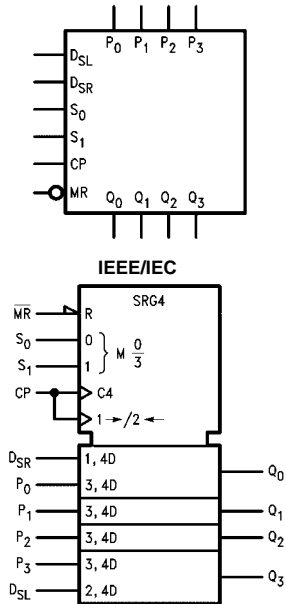
- Typical shift frequency of 150 MHz
- Asynchronous master reset
- Hold (do nothing) mode
- Fully synchronous serial or parallel data transfers

Ordering Code:

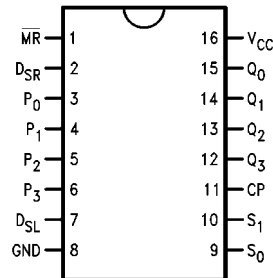
Order Number	Package Number	Package Description
74F194SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74F194PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
S ₀ , S ₁	Mode Control Inputs	1.0/1.0	20 μA/-0.6 mA
P ₀ -P ₃	Parallel Data Inputs	1.0/1.0	20 μA/-0.6 mA
D _{SR}	Serial Data Input (Shift Right)	1.0/1.0	20 μA/-0.6 mA
D _{SL}	Serial Data Input (Shift Left)	1.0/1.0	20 μA/-0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/-0.6 mA
$\overline{\text{MR}}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μA/-0.6 mA
Q ₀ -Q ₃	Parallel Outputs	50/33.3	-1 mA/20 mA

Functional Description

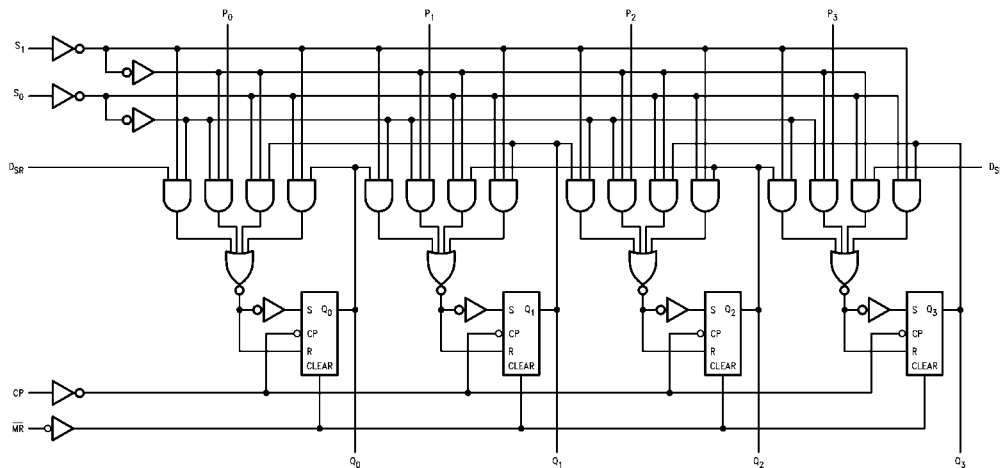
The 74F194 contains four edge-triggered D-type flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S₀, S₁) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data (P₀-P₃) and Serial data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset ($\overline{\text{MR}}$) overrides all other inputs and forces the outputs LOW.

Mode Select Table

Operating Mode	Inputs						Outputs			
	$\overline{\text{MR}}$	S ₁	S ₀	D _{SR}	D _{SL}	P _n	Q ₀	Q ₁	Q ₂	Q ₃
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q ₀	q ₁	q ₂	q ₃
Shift Left	H	h	l	X	l	X	q ₁	q ₂	q ₃	L
	H	h	l	X	h	X	q ₁	q ₂	q ₃	H
Shift Right	H	l	h	l	X	X	L	q ₀	q ₁	q ₂
	H	l	h	h	X	X	H	q ₀	q ₁	q ₂
Parallel Load	H	h	h	X	X	P _n	P ₀	P ₁	P ₂	P ₃

H (h) = HIGH Voltage Level
 L (l) = LOW Voltage Level
 p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
 X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

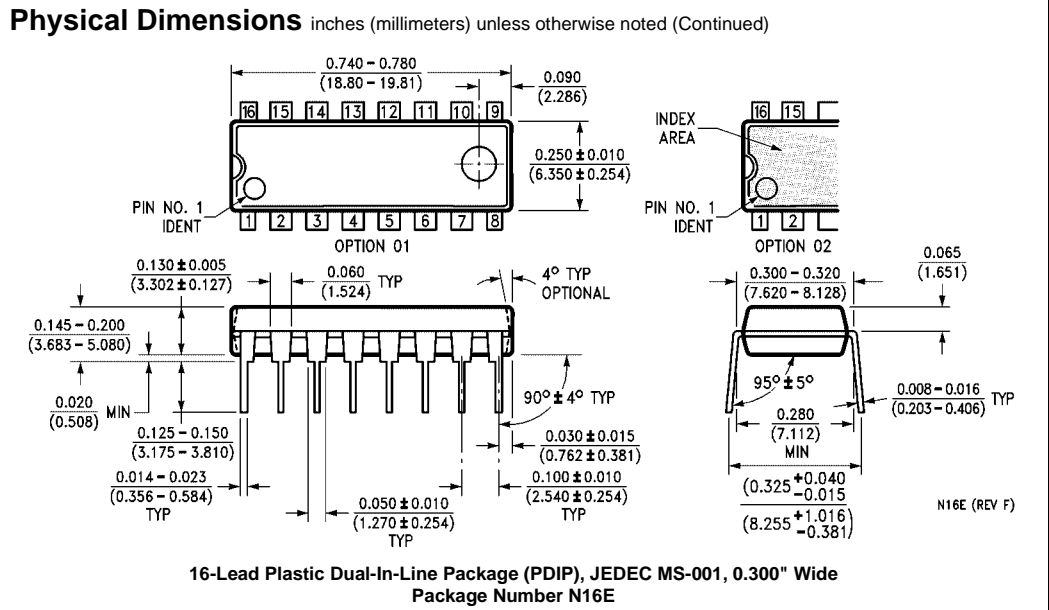
Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 5% V _{CC}	2.5 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5			I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current		33	46	mA	Max	

AC Electrical Characteristics									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Shift Frequency	105	150		90		90		MHz
t_{PLH}	Propagation Delay	3.5	5.2	7.0	3.0	8.5	3.5	8.0	ns
t_{PHL}	CP to Q_n	3.5	5.5	7.0	3.0	8.5	3.5	8.0	
t_{PHL}	Propagation Delay \overline{MR} to Q_n	4.5	8.6	12.0	4.5	14.5	4.5	14.0	ns
AC Operating Requirements									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		Units	
		Min	Max	Min	Max	Min	Max		
$t_{S(H)}$	Setup Time, HIGH or LOW	4.0		6.0		4.0		ns	
$t_{S(L)}$	P_n or D_{SR} or D_{SL} to CP	4.0		4.0		4.0			
$t_{H(H)}$	Hold Time, HIGH or LOW	1.0		1.5		1.0			
$t_{H(L)}$	P_n or D_{SR} or D_{SL} to CP	0		1.0		1.0		ns	
$t_{S(H)}$	Setup Time, HIGH or LOW	10.0		10.5		11.0			
$t_{S(L)}$	S_n to CP	8.0		8.0		8.0			
$t_{H(H)}$	Hold Time, HIGH or LOW	0		0		0		ns	
$t_{H(L)}$	S_n to CP	0		0		0			
$t_{W(H)}$	CP Pulse Width, HIGH	5.0		5.5		5.5		ns	
$t_{W(L)}$	\overline{MR} Pulse Width, LOW	5.0		5.0		5.0		ns	
t_{REC}	Recovery Time \overline{MR} to CP	9.0		9.0		11.0		ns	



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